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STIC EIC 2100
Search Request Form

Today's Date: | **What date would you like to use to limit the search?** Priority Date: | Other:

Name Trent Roche

AU 2124 | Examiner # 79908

Room # 5040 | Phone 305-4627

Serial # 09/883,710

Format for Search Results (Circle One):

(PAPER) DISK EMAIL

Where have you searched so far?

(USP) (DWPI) (EPO) (JPO) (ACM) (IBM TDB)

IEEE INSPEC SPI Other Citeseer

Is this a "Fast & Focused" Search Request? (Circle One) (YES) NO

A "Fast & Focused" Search is completed in 2-3 hours (maximum). The search must be on a very specific topic and meet certain criteria. The criteria are posted in EIC2100 and on the EIC2100 NPL Web Page at http://ptoweb/patents/stic/stic-tc2100.htm.

What is the topic, novelty, motivation, utility, or other specific details defining the desired focus of this search? Please include the concepts, synonyms, keywords, acronyms, definitions, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract, background, brief summary, pertinent claims and any citations of relevant art you have found.

A method for profiling code, consisting of branches & "stub" code. A stub in this context is a reference, or "forwarding" code, to an externally defined function or method. Note the definition at the top of page 3 of the spec. The system executes the code, generating profile + edge data. EACH Time it hits a stub, the starting "entry" point and target points of the stub are recorded in ~~data~~ a table. After execution, the profile + edge data is analyzed. If there is an edge which has a target attribute that matches a stub entry attribute in the stub table, then the edge target is assigned that matched stubs target.

STIC Searcher Renee Esterhold Phone 308-7795

Date picked up 6/21/04 9:45 am Date Completed 6/21/04 2:45 pm

sira Search and Information Resources Administration

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Set     Items   Description
S1         28   AU=(RAMASAMY, V? OR RAMASAMY V? OR HUNDT, R? OR HUNDT R?)
File 347:JAPIO Nov 1976-2004/Feb(Updated 040607)
         (c) 2004 JPO & JAPIO
File 348:EUROPEAN PATENTS 1978-2004/Jun W02
         (c) 2004 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20040617,UT=20040610
         (c) 2004 WIPO/Univentio
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200438
         (c) 2004  Thomson Derwent
```

1/5/17 **(Item 14 from file: 350)**
DIALOG(R)File 350:Derwent WPIX

015341202 **Image available**
WPI Acc No: 2003-402140/200338
XRPX Acc No: N03-320757

Computer implemented method for instrumentation of selected functions in executable program, involves obtaining relocation return pointer value associated with original return pointer value

Patent Assignee: GOURIOU E (GOUR-I); HUNDT R (HUND-I); RAMASAMY V (RAMA-I)
Inventor: GOURIOU E; **HUNDT R** ; **RAMASAMY V**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030037318	A1	20030220	US 2001930937	A	20010816	200338 B

Priority Applications (No Type Date): US 2001930937 A 20010816
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030037318	A1		8	G06F-009/44	

Abstract (Basic): US 20030037318 A1

NOVELTY - Relocation return pointer value associated with the original return pointer value is obtained and control is transferred to an instruction at the address referenced by the relocation return pointer value when breakpoint is encountered during the return of control at the original return pointer value.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for the apparatus for instrumentation of selected functions in an executable program.

USE - Computer implemented method for instrumentation of selected functions in executable program.

ADVANTAGE - Enables handling the return of control in calls by relocated and instrumented functions to other functions expecting a return pointer value in the original address space.

DESCRIPTION OF DRAWING(S) - The figure shows the flowchart explaining the process for the dynamic instrumentation of executable program code.

pp; 8 DwgNo 1/3

Title Terms: COMPUTER; IMPLEMENT; METHOD; INSTRUMENT; SELECT; FUNCTION; EXECUTE; PROGRAM; OBTAIN; RELOCATION; RETURN; POINT; VALUE; ASSOCIATE; ORIGINAL; RETURN; POINT; VALUE
Derwent Class: T01
International Patent Class (Main): G06F-009/44
File Segment: EPI

1/5/18 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015280506 **Image available**
WPI Acc No: 2003-341437/200332
XRPX Acc No: N03-273116

Computer-implemented program optimizing method involves replacing target address of identified branch instructions with predetermined address provided for implementing predefined function

Patent Assignee: HUNDT R (HUND-I); RAMASAMY V (RAMA-I)
Inventor: **HUNDT R ; RAMASAMY V**

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030009750	A1	20030109	US 2001901363	A	20010709	200332	B

Priority Applications (No Type Date): US 2001901363 A 20010709
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030009750	A1		8	G06F-009/45	

Abstract (Basic): US 20030009750 A1

NOVELTY - The branch instructions having target address that references the linkage stub code segment, are identified. The target address of the branch instructions, is replaced with an address at which predefined function is implemented.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for apparatus for optimizing executable program.

USE - For optimizing executable computer programs in computer system.

ADVANTAGE - Since the target address is replaced with address of code implementing the function, the invoking of function several times during program execution is reduced. Thus, significant amount of time spending to execute linkage stub function is reduced. Eliminates path through the linkage stub functions, due to dynamic optimization of program, thus the performance of executable program code is improved.

DESCRIPTION OF DRAWING(S) - The figure shows a flowchart explaining the method for dynamic optimization of executable program code having linkage stub functions.

pp; 8 DwgNo 2/3

Title Terms: COMPUTER; IMPLEMENT; PROGRAM; OPTIMUM; METHOD; REPLACE; TARGET ; ADDRESS; IDENTIFY; BRANCH; INSTRUCTION; PREDETERMINED; ADDRESS; IMPLEMENT; PREDEFINED; FUNCTION
Derwent Class: T01
International Patent Class (Main): G06F-009/45
File Segment: EPI

1/5/19 (Item 16 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015227802 **Image available**
WPI Acc No: 2003-288715/200328
XRPX Acc No: N03-229546

Computer-based edge profile data generation method involves identifying entry point address and target addresses of stub code segment for matching with edges for changing edge target attribute

Patent Assignee: HUNDT R (HUND-I); RAMASAMY V (RAMA-I)
Inventor: **HUNDT R ; RAMASAMY V**

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020194580	A1	20021219	US 2001883710	A	20010618	200328 B

Priority Applications (No Type Date): US 2001883710 A 20010618
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020194580	A1		8	G06F-009/44	

Abstract (Basic): US 20020194580 A1

NOVELTY - The edges representing branch instruction in executable program code, is created and associated with source, target and edge count attributes. The number of execution of branch instruction are counted for assigning values to edge count attributes. Entry point address and target addresses of stub code segment are identified for matching with edges for changing edge target attribute.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for edge profile data generating apparatus.

USE - For generating edge profile data for executable program code.

ADVANTAGE - The correlation of execution profile information with source code is performed easily by identifying entry point address and target point address of stub code segment.

DESCRIPTION OF DRAWING(S) - The figure shows the flowchart explaining the method of generating edge profile data.

pp; 8 DwgNo 3/4

Title Terms: COMPUTER; BASED; EDGE; PROFILE; DATA; GENERATE; METHOD; IDENTIFY; ENTER; POINT; ADDRESS; TARGET; ADDRESS; STUB; CODE; SEGMENT; MATCH; EDGE; CHANGE; EDGE; TARGET; ATTRIBUTE
Derwent Class: T01
International Patent Class (Main): G06F-009/44
File Segment: EPI

1/5/20 (Item 17 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015227609 **Image available**
WPI Acc No: 2003-288522/200328
XRPX Acc No: N03-229353

Computer program optimization method involves relocating calling code segments and target code segments to new address and replacing their references suitably according to new address

Patent Assignee: HUNDT R (HUND-I); RAMASAMY V (RAMA-I)
Inventor: **HUNDT R ; RAMASAMY V**

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020188932	A1	20021212	US 2001876655	A	20010607	200328	B

Priority Applications (No Type Date): US 2001876655 A 20010607
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020188932	A1		10	G06F-009/45	

Abstract (Basic): US 20020188932 A1

NOVELTY - Address-bridging code segments, target and calling code segments are identified during program execution. The calling and the target code segments are relocated to a new address. References to address-bridging code segments, are replaced to that of relocated target code segments. References for calling code segments in the initial address, are directed to the relocated calling code segments.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for computer program optimization apparatus.

USE - For optimization of computer program having address-bridging code segments.

ADVANTAGE - Since the calling code segments directly branch to the target code segments due to code relocation, address-bridging codes are eliminated and hence the processor time to execute the address-bridging codes is avoided.

DESCRIPTION OF DRAWING(S) - The figure shows the flowchart explaining the address-bridging code optimization process.

pp; 10 DwgNo 3/5

Title Terms: COMPUTER; PROGRAM; OPTIMUM; METHOD; RELOCATION; CALL; CODE; SEGMENT; TARGET; CODE; SEGMENT; NEW; ADDRESS; REPLACE; REFERENCE; SUIT; ACCORD; NEW; ADDRESS
Derwent Class: T01
International Patent Class (Main): G06F-009/45
File Segment: EPI

Set	Items	Description
S1	81002	(PROFILE OR EDGE? OR MODULE? OR NODE? OR VERTICE? OR VERTEX OR EDGES OR ATOMIC()PROPOSITION? OR ADDRESSABLE()DEVICE? OR -SET OR SUBSET OR SUB()SET?)(2N)(CODE OR CODES OR INFORMATION -OR DATA)
S2	4167	(BRANCH? OR LEAF OR LEAVES OR STUB OR STUBS OR ROUTINE? OR REFERENCE OR FORWARDING)(N)(CODE OR CODES OR INSTRUCTION?)
S3	31591	(EXTERNAL? OR OUTSIDE OR OUT()SIDE OR EXTERIOR? OR INDEPEN-DENT?)(2N)(FUNCTION? OR METHOD? OR INSTRUCTION? OR OPERATION? OR EXECUTION? OR COMMAND?)
S4	11412	(EXECUT? OR PERFORM? OR TRANSACT?)(3N)CODE? ?
S5	5681257	GENERAT? OR CREAT? OR PRODUC? OR DEVELOP? OR ESTABLISH?
S6	5374755	CONNECT? OR LINK? OR JOIN? OR UNITE? OR UNIFY OR UNIFIES OR COMBINE? OR ASSOCIAT? OR AFFILIAT? OR ASSEMBLE? OR TIE? OR C-OLLECT?
S7	35470	(PROFILE? OR HISTOR? OR PATTERN? OR ATTRIBUT? OR EDGE)(2N)-DATA
S8	1240467	HIT OR HITS OR LOCAT? OR FIND? OR MATCH?
S9	28315	(OPEN? OR START? OR BEGIN? OR ENTRY)(N)POINT?
S10	6839	(TARGET? OR INDICAT? OR GOAL? OR DESTINATION)(N)(POINT? OR ATTRIBUT?)
S11	2404993	REGISTER? OR RECORD? OR LIST? OR PRESERV? OR SAVE? OR SAVI-NG OR KEEP? OR WRITE? OR POST? OR LOG OR LOGGED OR LOGGING OR ENTER? ? OR ENTERING
S12	1339808	TABLE? OR TUPLE? OR ROW? OR MATRIX OR MATRICES OR ARRAY? OR COLUMN? OR GRID? OR GRAPH? OR (MATHEMATICAL OR DATA)()ELEMEN-T?
S13	27216	(AFTER OR SUBSEQUENT OR LATER OR FOLLOWING OR SUCCEEDING OR SUCCESSIVE OR SEQUENT)(N)(EXECUT? OR PERFORM? OR TRANSACT?)
S14	3892352	ANALYZ? OR ANALYS? OR COMPAR? OR MATCH? OR VERI? OR ANALYZ? OR ANALYS? OR LINK? OR SYNCHRON? OR CONFORM? OR AGREE? OR CO-MPLIANT OR COMPATIBLE OR DIFFERENT? OR DIFFERENCE? OR SIMILAR? OR DISTINGUISH? OR DISCRIMINAT?
S15	847680	MARKER?()BIT? OR INDICAT? OR TAG OR TAGS OR TAGGED OR TAGG-ING OR MAPPING OR MAP OR MAPS OR TARGET?
S16	27	S1 AND (S2 OR S3) AND S4
S17	1	S1 AND S2 AND S3 AND S4
S18	8	S1 AND S2 AND S3
S19	34	S16 OR S17 OR S18
S20	29	S19 AND IC=G06F?

File 347:JAPIO Nov 1976-2004/Feb(Updated 040607)
(c) 2004 JPO & JAPIO
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200438
(c) 2004 Thomson Derwent

20/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06890381 **Image available**
DEVICE AND METHOD FOR COMPILING PARALLEL CONVERSION AND RECORDING MEDIUM FOR RECORDING PARALLEL CONVERSION

PUB. NO.: 2001-117890 [JP 2001117890 A]
PUBLISHED: April 27, 2001 (20010427)
INVENTOR(s): OBATA MASAYA
APPLICANT(s): NEC CORP
APPL. NO.: 11-301316 [JP 99301316]
FILED: October 22, 1999 (19991022)
INTL CLASS: **G06F-015/16 ; G06F-009/45**

ABSTRACT

PROBLEM TO BE SOLVED: To prepare a target **code** or **executing** a preceding processing which starts from a jump destination in parallel, where control is moved by a high probability without re-arranging basic blocks.

SOLUTION: A system is provided with a branch duplex part for judging the truth or falsehood probability of a evaluation value in a condition formula concerning a condition **branch instruction** in an intermediate **code** based on **profile information**, executing duplexing into a condition **branch instruction** where the jump destination is changed to be at the position of a succeeding instruction by inverting the formula and into the instruction obtained by permitting the condition **branch instruction** to be a non-condition **branch instruction** as it is in the case of a high falsehood probability and executing duplexing into the instruction obtained by outputting the condition **branch instruction** as it is and into the non-condition **branch instruction** where the position of the succeeding instruction of the condition **branch instruction** is adopted as the jump destination in the case of a high truth probability. Besides, the system is provided with a branch inverting part for preparing the target code corresponding to the intermediate code were the jump destination of the condition **branch instruction** and the jump destination of the non-condition **branch instruction** are exchanged when the judgement of the truth or falsehood probability based on **profile information** is inverted compared with the one when the target code is prepared.

20/5/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

05545811 **Image available**
PROGRAMMABLE CONTROLLER

PUB. NO.: 09-160611 [JP 9160611 A]
PUBLISHED: June 20, 1997 (19970620)
INVENTOR(s): TAMURA FUMIYUKI
FUJIWARA KATSUHIRO
AIDA NORIHIRO
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 07-316570 [JP 95316570]
FILED: December 05, 1995 (19951205)
INTL CLASS: [6] G05B-019/05; **G06F-009/06 ; G06F-009/06**
JAPIO CLASS: 22.3 (MACHINERY -- Control & Regulation); 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessers)

ABSTRACT

(Japan)
APPL. NO.: 03-238778 [JP 91238778]
FILED: August 26, 1991 (19910826)
INTL CLASS: [5] **G06F-009/45** ; **G06F-009/445**
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JOURNAL: Section: P, Section No. 1570, Vol. 17, No. 363, Pg. 97, July 08, 1993 (19930708)

ABSTRACT

PURPOSE: To improve speed for executing a program and link speed.

CONSTITUTION: In the case of compile, an **external function** calling **instruction** generating means 11 generates the pair of a NOP instruction and a direct calling instruction in respect to an **external function** calling **instruction** . An **external function** pointer **reference instruction** generating means 12 generates a normal **reference instruction** in respect to an **external function** pointer **reference instruction** and sets information showing reference to a symbol table 51. In the case of static link, a load module inside unresolved **external function** resolving means 21 executes a relocation processing by executing the static link to an **external function** referred to as a function pointer and when no **information** is **set** , the part of the **external function** calling **instruction** is reloaded with an instruction for activating a dynamic linker. In respect to the instruction, partial segment information 62 is defined. In the case of generating a process, a segment mapping means 31 receives the partial segment information 62 and generates a partially writable text segment. In the case of execution, a text reloading means 42 reloads the instruction for activating the dynamic linker with the **external function** calling **instruction** .

20/5/5 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

03821331 **Image available**
DATA PROCESSOR

PUB. NO.: 04-186431 [JP 4186431 A]
PUBLISHED: July 03, 1992 (19920703)
INVENTOR(s): NOGUCHI YOSHIKI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-313995 [JP 90313995]
FILED: November 21, 1990 (19901121)
INTL CLASS: [5] **G06F-009/32** ; **G06F-009/22** ; **G06F-015/78**
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units); 45.4 (INFORMATION PROCESSING -- Computer Applications)
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessers)
JOURNAL: Section: P, Section No. 1441, Vol. 16, No. 511, Pg. 80, October 21, 1992 (19921021)

ABSTRACT

PURPOSE: To rapidly change a processing sequence based upon externally inputted code information by setting up an optional logical **function** in the **externally** inputted code information and directly using the function value as a condition for a **branch instruction** .

CONSTITUTION: Code information stored in a storage means 1 is divided into plural data respectively having a prescribed bit length and the divided data are respectively inputted to means 2, 3 for executing specified logical function operation. Since all logical functions can be specified to the data with the prescribed bit length by using other code information with the prescribed bit length, an optional logical function can be set up in the input code information. The operation results of respective divided data by optional logical functions are outputted as one signal output by a

logical operation means 4 and the signal output is directly used by a means 6 as a branch condition for a **branch instruction** . Thus a response speed required in the case of changing a processing sequence based upon an externally inputted code **information** can be **set** up to a rapid speed.

20/5/6 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

03239440 **Image available**
METHOD EXECUTING SYSTEM

PUB. NO.: 02-214940 [JP 2214940 A]
PUBLISHED: August 27, 1990 (19900827)
INVENTOR(s): ONO MIYUKI
ONO KOSHIO
TORII SATORU
YANAGI TOMOKO
HAGIWARA TSUNEKO
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-036696 [JP 8936696]
FILED: February 16, 1989 (19890216)
INTL CLASS: [5] **G06F-009/44**
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JOURNAL: Section: P, Section No. 1130, Vol. 14, No. 516, Pg. 18, November 13, 1990 (19901113)

ABSTRACT

PURPOSE: To reduce the method executing load by preparing a method **code module** , a method table, and a coupled **method** module **independently** of each other.

CONSTITUTION: The **code modules** 3 are produced for the methods defined in the classes respectively. At the same time, the pointers are registered to point the method name in its own class, the method name of the class to be succeeded and capable of solution of the succession, and the **execution code set** in the corresponding module 3 respectively to the method tables 1 and the coupled method module 2 set for each class. Then the methods of the succession classes or unsolved or changed classes are registered in the tables 1 and the module 2 or changed by reference to the tables 1 and the module 2 at **execution** of the **execution codes** stored in the modules 3. Thus the succession of the class is solved and executed. As a result, the succession is solved and executed as necessary and at the same time the succession class can be easily changed.

20/5/7 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO

02623728 **Image available**
GRAPHIC SUBSYSTEM CONTROL SYSTEM

PUB. NO.: 63-240628 [JP 63240628 A]
PUBLISHED: October 06, 1988 (19881006)
INVENTOR(s): SHIMOMURA TSUTOMU
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-074831 [JP 8774831]
FILED: March 28, 1987 (19870328)
INTL CLASS: [4] **G06F-009/06** ; **G06F-003/14**
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units); 45.3 (INFORMATION PROCESSING -- Input Output Units)
JAPIO KEYWORD:R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessers)

JOURNAL: Section: P, Section No. 822, Vol. 13, No. 47, Pg. 41, February 03, 1989 (19890203)

ABSTRACT

PURPOSE: To omit the interruption to a main CPU and to perform the complicated processing via the combination of simple commands, by carrying out not only the single command processing but combining plural commands to carry out the processing in a command train.

CONSTITUTION: Plural processors 12 are provided which can give the interruption requests to each other and also can control the permission and inhibition of interruptions based on the **information set** previously. A memory 13 stores the commands which receive accesses from those processors 12 and a memory 15 stores the stored positions of these **commands** . Then, the **independent commands** which are capable of execution with plural command trains are provided together with such commands containing control instructions to the command trains of condition waiting **instructions** , **branch instructions** , etc. Thus, an interruption can be omitted to a main CPU 1 and the overhead due to an interruption is eliminated. As a result, the complicated processing is possible with the combination of simple commands.

20/5/8 (Item 8 from file: 347)

02461343 **Image available**

LOGICAL SIMULATION SYSTEM FOR MICROCOMPUTER

PUB. NO.: 63-078243 [JP 63078243 A]
PUBLISHED: April 08, 1988 (19880408)
INVENTOR(s): NAKAMAE MIDORI
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-222147 [JP 86222147]
FILED: September 22, 1986 (19860922)
INTL CLASS: [4] **G06F-011/26**
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JAPIO KEYWORD:R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessers)
JOURNAL: Section: P, Section No. 748, Vol. 12, No. 309, Pg. 8, August 23, 1988 (19880823)

ABSTRACT

PURPOSE: To shorten a logical simulation period without needing a labor by sing a port control signal outputted from a CPU and setting successively data to an input port.

CONSTITUTION: A test program 3a of a new form is converted to an instruction code and converted to a logical simulation command. Port data in the test program 3a are converted to a command to store into a port ROM 7. When these commands are inputted to a logical simulation object circuit 10 and a logical simulation is **executed** , an instruction **code** is stored into an external ROM 2, port data are stored into the port ROM 7, and by giving a resetting signal, the **instruction** in the **external** ROM 2 is executed. When the instruction is a port input instruction, a CPU 1d generates a port control signal 1f(sub a), inputs it to a counter circuit 8, outputs an address for a port ROM, and therefore, the **data** are **set** to an input port 1a.

20/5/9 (Item 9 from file: 347)

01631543 **Image available**

INFORMATION PROCESSOR

PUB. NO.: 60-110043 [JP 60110043 A]
PUBLISHED: June 15, 1985 (19850615)
INVENTOR(s): NISHIKAWA TAKESHI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 58-217980 [JP 83217980]
FILED: November 18, 1983 (19831118)
INTL CLASS: [4] **G06F-009/32**
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JOURNAL: Section: P, Section No. 398, Vol. 09, No. 262, Pg. 8, October 19, 1985 (19851019)

ABSTRACT

PURPOSE: To execute conditional branching with high flexibility and at a high speed by designating optionally with an instruction one of plural condition code memory means to which the **information** is **set** together with readout of said information.

CONSTITUTION: A process B is first **executed** and a condition **code** register is designated to **set** the condition **code** produced by the processing which is executed by a CCRP field of an instruction word. Then the condition **code** is **set** to a condition code register CCR0 by the process B. Then a process A is executed to set the produced condition code to a register CCR1. At the same time, the CCR1 is designated by the subsequent first **branching instruction** . Then the conditional branching of the process A is executed. Finally the CCR1 storing the condition code of the process B is designated by the 2nd **branching instruction** . Then the conditional branching corresponding to said condition **code** is **executed** .

20/5/10 (Item 1 from file: 350)

015834157 **Image available**
WPI Acc No: 2003-896361/200382
XRPX Acc No: N03-715280

Computer program code executing **system, has processing circuitry to execute unconditional** branch instruction **based on mode indicator when code is disabled and refrains from instruction, and** executing code **when** code **is enabled**

Patent Assignee: HEWLETT-PACKARD DEV CO LP (HEWP)
Inventor: HUCK J; THOMPSON C L
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6654877	B1	20031125	US 2000644435	A	20000823	200382	B

Priority Applications (No Type Date): US 2000644435 A 20000823
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6654877	B1		10	G06F-009/44	

Abstract (Basic): US 6654877 B1

NOVELTY - The system has a processing circuitry (32) that receives run time data indicating whether a **set** of **codes** is enabled or disabled. A value of a mode indicator (71) is set based on the data. The circuitry executes an unconditional **branch instruction** based on the indicator when the code is disabled and refrains to execute the instruction based on the indicator. The circuitry **executes** the **set** of **code** on enabling.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of selectively **executing** sets of **code** in computer programs.

USE - Used for selectively **executing** sets of **code** in a computer program.

ADVANTAGE - The presence of the disabled code in the program does not affect the performance of the program since the **execution** of the **code** is based on the status of the mode indicator. The circuitry executes unconditional **branch** **instruction** based on the mode indicator, thereby preventing execution of the **set** of **code** when the code is disabled.

DESCRIPTION OF DRAWING(S) - The drawing shows a block diagram of a processing circuitry in a computer system.

Processing circuitry (32)
Mode indicator (71)
Instruction dispersal unit (75)
Control circuitry (77)
Pipelines (79)
pp; 10 DwgNo 3/4

Title Terms: COMPUTER; PROGRAM; CODE; EXECUTE; SYSTEM; PROCESS; CIRCUIT; EXECUTE; UNCONDITIONAL; BRANCH; INSTRUCTION; BASED; MODE; INDICATE; CODE; DISABLE; INSTRUCTION; EXECUTE; CODE; CODE; ENABLE
Derwent Class: T01
International Patent Class (Main): **G06F-009/44**
International Patent Class (Additional): **G06F-009/45** ; **G06F-011/36**
File Segment: EPI

20/5/11 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015227802 **Image available**
WPI Acc No: 2003-288715/200328
XRPX Acc No: N03-229546

Computer-based edge profile data **generation method involves identifying entry point address and target addresses of** stub code **segment for matching with edges for changing edge target attribute**

Patent Assignee: HUNDT R (HUND-I); RAMASAMY V (RAMA-I)
Inventor: HUNDT R; RAMASAMY V
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020194580	A1	20021219	US 2001883710	A	20010618	200328	B

Priority Applications (No Type Date): US 2001883710 A 20010618
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020194580	A1		8	G06F-009/44	

Abstract (Basic): US 20020194580 A1

NOVELTY - The edges representing **branch** **instruction** in **executable** program **code** , is created and associated with source, target and edge count attributes. The number of execution of **branch** **instruction** are counted for assigning values to edge count attributes. Entry point address and target addresses of **stub** **code** segment are identified for matching with edges for changing edge target attribute.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for **edge** **profile** **data** generating apparatus.

USE - For generating **edge** **profile** **data** for **executable** program **code** .

ADVANTAGE - The correlation of execution **profile** **information** with source **code** is **performed** easily by identifying entry point address and target point address of **stub** **code** segment.

DESCRIPTION OF DRAWING(S) - The figure shows the flowchart explaining the method of generating **edge** **profile** **data** .

pp; 8 DwgNo 3/4

Title Terms: COMPUTER; BASED; EDGE; PROFILE; DATA; GENERATE; METHOD; IDENTIFY; ENTER; POINT; ADDRESS; TARGET; ADDRESS; STUB; CODE; SEGMENT; MATCH; EDGE; CHANGE; EDGE; TARGET; ATTRIBUTE
Derwent Class: T01
International Patent Class (Main): **G06F-009/44**

clusters of predetermined equal size in the vector space of a fixed number of dimensions.

USE - The method is used for determination of a biological state such as a disease, stage of disease, prognosis of disease, disease of the internal body organ, stage of the disease of the internal body organ, health of the internal body organ, toxicity and relative toxicity of chemical(s), efficacy of the drug(s), responsiveness to a regimen of therapy, state of perturbation of a body organ and presence of at least one pathogen; e.g. in the diagnosis of diseases such as autoimmune diseases, Alzheimer's disease, arthritis, glomerulonephritis, infectious disease and cancer such as primary malignancy, carcinomas e.g. prostatic and ovarian carcinoma, melanoma, lymphoma, sarcoma, blastoma, leukemia, myeloma, neutral tumor (claimed).

ADVANTAGE - The discriminatory patterns are new and can be defined without any knowledge of the identity or relationship between the individual data points in the biological data or any knowledge of the identity or relationship between the molecules in the biological samples. The method discovers optimal hidden molecular patterns as subsets within a larger complex data field, such that the pattern itself is discriminatory between biological states, without involving the difficult and time consuming analytical methods associated with the prior art.

pp; 48 DwgNo 0/0

Title Terms: CLASSIFY; BIOLOGICAL; STATE; BIOLOGICAL; DATA; USEFUL; DIAGNOSE; DISEASE; CANCER; COMPRISE; DETECT; DISCRIMINATE; PATTERN; APPLY ; PATTERN; CLASSIFY; UNKNOWN; DATA; SAMPLE

Derwent Class: B03; B04; D16; K08; P31; S03

International Patent Class (Main): G01N-033/48; **G06F-019/00**

International Patent Class (Additional): A61B-005/00; C12Q-001/68; G01N-033/50

File Segment: CPI; EPI; EngPI

20/5/13 (Item 4 from file: 350)

DIALOG(R)File 350:Derwent WPIX

013855444 **Image available**

WPI Acc No: 2001-339657/200136

XRPX Acc No: N01-245641

Software development management assistance system in computer, edits stored source and module **execution** information **, and displays it on display device**

Patent Assignee: HITACHI JOHO SYSTEMS KK (HITA-N)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2001092650	A	20010406	JP 99271421	A	19990924	200136	B

Priority Applications (No Type Date): JP 99271421 A 19990924

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2001092650	A		12	G06F-009/06	

Abstract (Basic): JP 2001092650 A

NOVELTY - Source information is extracted from compiled source program (211). Test **execution** of **code** which calls **external** library **function** , is performed to extract **module** execution **information** (216). Receiving unit (220) of management computer (25) receives extracted source and **module** execution **information** from development computer (21), and stores in database (221). The stored information is edited and displayed.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) Software development management assistance procedure;

(b) Recording medium

USE - For assisting management of software development in computer systems.

ADVANTAGE - Enables performing exact and efficient management of progress situation of software development operation.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of software development management assistance system. (Drawing includes non-English language text).

Development computer (21)
Management computer (25)
Source program (211)
Module execution **information** (216)
Receiving unit (220)
Database (221)
pp; 12 DwgNo 1/7

Title Terms: SOFTWARE; DEVELOP; MANAGEMENT; ASSIST; SYSTEM; COMPUTER; EDIT; STORAGE; SOURCE; MODULE; EXECUTE; INFORMATION; DISPLAY; DISPLAY; DEVICE
Derwent Class: T01
International Patent Class (Main): **G06F-009/06**
File Segment: EPI

20/5/14 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013808889 **Image available**
WPI Acc No: 2001-293101/200131
XRPX Acc No: N01-209623

Parallelizing compilation apparatus inverts conditional expression or generates branch instruction **depending on conditional expression evaluation value probability**

Patent Assignee: NEC CORP (NIDE)
Inventor: OBATA M
Number of Countries: 026 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1094387	A2	20010425	EP 2000122314	A	20001020	200131	B
JP 2001117890	A	20010427	JP 99301316	A	19991022	200141	

Priority Applications (No Type Date): JP 99301316 A 19991022
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1094387	A2	E	24	G06F-009/45	
				Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI	
JP 2001117890	A		16	G06F-015/16	

Abstract (Basic): EP 1094387 A2

NOVELTY - System comprises a section (12) for analyzing the source program (11), **profile information** store (17), branch determining section (18) and section (13) which replaces a conditional **branch instruction** included in the codes with another conditional **branch instruction** as a first **branch instruction** in which the branch target points to the processing that begins at the branch target, where the conditional **branch instruction branches** with higher probability, and an unconditional **branch instruction** as a second **branch instruction** in which the branch target points to the processing that begins at the branch target where the conditional **branch instruction branches** with lower probability. It also has a parallel optimizer (14) and **profile information** history store (18), plus branch inverter (19).

DETAILED DESCRIPTION - There are INDEPENDENT CLAIMS for (1) a parallelizing compilation method and (2) a parallelizing compilation program.

USE - Apparatus is for generating object **codes** for **execution** of parallel processor processes.

ADVANTAGE - Apparatus generates object **codes** for **executing**

20/5/17 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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012890000 **Image available**
WPI Acc No: 2000-061834/200005
Related WPI Acc No: 1999-580061
XRPX Acc No: N00-048512
Machine executable code **optimization method for conversion of computer programs**
Patent Assignee: DIGITAL EQUIP CORP (DIGI)
Inventor: SRIVASTAVA A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5999737	A	19991207	US 94204833	A	19940301	200005	B
			US 96752728	A	19961119		
			US 97963087	A	19971103		

Priority Applications (No Type Date): US 94204833 A 19940301; US 96752728 A 19961119; US 97963087 A 19971103
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5999737	A		19	G06F-009/44	Cont of application US 94204833
					Cont of application US 96752728

Abstract (Basic): US 5999737 A
NOVELTY - Object **code modules** compiled from a **set** of source **code module** of high level language, is translated into a linked **code module** in form of intermediate language. Machine **executable code** compatible to target computer system architecture, is generated from the linked **code modules** .
DETAILED DESCRIPTION - The intermediate language has **instruction independent** of hardware architecture of a computer system. The linked **code module** is modified to optimize **execution** of machine executable **code** . A first **set** of instruction which are not executed and a second set of instructions which compute unused values, are detected from linked **code module** .
USE - For conversion of computer programs.
ADVANTAGE - Reduces number of register to be used for optimization of **executable code** , and ensures full utilization of memory and registers during execution.
DESCRIPTION OF DRAWING(S) - The figure shows top level flow diagram for machine **executable code** optimization.
pp; 19 DwgNo 2/9
Title Terms: MACHINE; EXECUTE; CODE; METHOD; CONVERT; COMPUTER; PROGRAM
Derwent Class: T01
International Patent Class (Main): **G06F-009/44**
File Segment: EPI

20/5/18 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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012773834 **Image available**
WPI Acc No: 1999-580061/199949
Related WPI Acc No: 2000-061834
XRPX Acc No: N99-428242
Machine executable code **optimization method for computer system**
Patent Assignee: DIGITAL EQUIP CORP (DIGI)
Inventor: SRIVASTAVA A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5966539	A	19991012	US 94204833	A	19940301	199949	B
			US 95514368	A	19950811		

US 96748606 A 19961113
US 97963086 A 19971103

Priority Applications (No Type Date): US 94204833 A 19940301; US 95514368 A 19950811; US 96748606 A 19961113; US 97963086 A 19971103
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5966539	A		19	G06F-009/44	Cont of application US 94204833 Cont of application US 95514368 Cont of application US 96748606

Abstract (Basic): US 5966539 A

NOVELTY - Compiled object **code modules** from source **codes** are generated as machine **executable codes** which are translated into intermediate language of intermediate program code with **independent instructions** of particular computer system hardware architecture. Then, machine dependent **executable code** is generated, which is compatible with target computer system hardware architecture.

USE - For computer system using compiler, linker, assembler.

ADVANTAGE - Optimizes linked code before machine **code** generation. Each **set** of variables are analyzed and thus used to remove dead code from the linked **code** . **Execution** time of loops are minimized by moving intra-procedural and inter-procedural loop invariant code across procedure boundaries.

DESCRIPTION OF DRAWING(S) - The figure shows flow diagram of procedure optimized machine **executable code** for computer system.

pp; 19 DwgNo 2/9

Title Terms: MACHINE; EXECUTE; CODE; METHOD; COMPUTER; SYSTEM
Derwent Class: T01
International Patent Class (Main): **G06F-009/44**
File Segment: EPI

20/5/19 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012574987 **Image available**
WPI Acc No: 1999-381094/199932
XRPX Acc No: N99-285837

Condition branch or multi- branch instruction optimization system in compiler - generates control flow graph showing relationship of basic block of intermediate language generated based on source program

Patent Assignee: FUJITSU LTD (FUIT)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 11149381	A	19990602	JP 97317921	A	19971119	199932	B

Priority Applications (No Type Date): JP 97317921 A 19971119
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11149381	A		14	G06F-009/45	

Abstract (Basic): JP 11149381 A

NOVELTY - A graph generator (43) generates a control flow graph showing relationship of basic block of an intermediate language generated based on source program. An information generator (4) obtains execution frequency or execution probability of basic block of a control flow graph. A processor (5) performs optimization, based on **profile information** and control flow graph. DETAILED DESCRIPTION - A block detector (11) detects a basic block to be optimized, based on **profile information** . A copy of the basic block and optimized control flow graph are generated such that a deviation occurs to an **execution** frequency. **INDEPENDENT** CLAIMS are also included for the following: memory medium which stores executable program; executable program generation method

branches to the relatively simple branch predictor.
USE - Identifying hard-to-predict branches in e.g. deeply pipelined, out-of-order execution processors.
ADVANTAGE - Improves performance of computer systems executing programs having **branch instructions** .
Dwg.1/5
Title Terms: BRANCH; INSTRUCTION; HANDLE; METHOD; PROCESS; SOURCE; PROGRAM; PRODUCE; MACHINE; EXECUTE; CODE; SET; APPLY; CLASSIFY; BRANCH; INSTRUCTION; HARD; PREDICT; SIMPLE; BRANCH
Derwent Class: T01
International Patent Class (Main): **G06F-009/00**
International Patent Class (Additional): **G06F-009/06**
File Segment: EPI

20/5/21 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010896615 **Image available**
WPI Acc No: 1996-393566/199639
XRPX Acc No: N96-331592
Speculative instruction execution tracking for processor - involves assigning identification tag to each instruction issued with associated activity bit set on issue and cleared on completion
Patent Assignee: FUJITSU LTD (FUIT); HAL COMPUTER SYSTEMS INC (HALC-N)
Inventor: MARUYAMA T; OSONE H; PATKAR N A; SHEBANOW M C; SHEN G W; SIMONE M A; SZETO J
Number of Countries: 020 Number of Patents: 013
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9625705	A1	19960822	WO 96US1930	A	19960213	199639	B
US 5644742	A	19970701	US 95390885	A	19950214	199732	
			US 95398299	A	19950303		
			US 95473223	A	19950607		
US 5649136	A	19970715	US 95390885	A	19950214	199734	
			US 95398299	A	19950303		
			US 95483958	A	19950607		
US 5651124	A	19970722	US 95390885	A	19950214	199735	
			US 95398299	A	19950303		
			US 95478025	A	19950607		
US 5655115	A	19970805	US 95390885	A	19950214	199737	
			US 95398299	A	19950303		
			US 95482075	A	19950607		
US 5659721	A	19970819	US 95390885	A	19950214	199739	
			US 95398299	A	19950303		
			US 95476419	A	19950607		
US 5673408	A	19970930	US 95390885	A	19950214	199745	
			US 95398299	A	19950303		
			US 95472394	A	19950607		
US 5673426	A	19970930	US 95390885	A	19950214	199745	
			US 95398299	A	19950303		
			US 95484795	A	19950607		
EP 815507	A1	19980107	EP 96906404	A	19960213	199806	
			WO 96US1930	A	19960213		
US 5751985	A	19980512	US 95390885	A	19950214	199826	
			US 95398299	A	19950303		
			US 95487801	A	19950607		
JP 11500551	W	19990112	JP 96525085	A	19960213	199912	
			WO 96US1930	A	19960213		
KR 98702203	A	19980715	WO 96US1930	A	19960213	199927	
			KR 97705598	A	19970813		
US 5966530	A	19991012	US 95390885	A	19950214	199949	
			US 95398299	A	19950303		
			US 95487801	A	19950607		
			US 97872982	A	19970611		

Priority Applications (No Type Date): US 95487801 A 19950607; US 95390885 A 19950214; US 95398299 A 19950303; US 95472394 A 19950607; US 95473223 A 19950607; US 95476419 A 19950607; US 95478025 A 19950607; US 95482073 A 19950607; US 95483958 A 19950607; US 95484795 A 19950607; US 95482075 A 19950607; US 97872982 A 19970611

Cited Patents: 05 26901700; 05 35545700; 05 46374500; 05 47159800; 05 48168500; 5497499

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9625705	A1	E	245	G06F-009/00	
Designated States (National): JP KP KR US					
Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE					
US 5644742	A		107	G06F-011/00	Cont of application US 95390885
					Cont of application US 95398299
US 5649136	A		108	G06F-011/00	Cont of application US 95390885
					Cont of application US 95398299
US 5651124	A		112	G06F-011/00	Cont of application US 95390885
					Cont of application US 95398299
US 5655115	A		122	G06F-009/38	Cont of application US 95390885
					Cont of application US 95398299
US 5659721	A		112	G06F-011/00	Cont of application US 95390885
					Cont of application US 95398299
US 5673408	A		111	G06F-009/00	Cont of application US 95390885
					Cont of application US 95398299
US 5673426	A		109	G06F-007/46	Cont of application US 95390885
					Cont of application US 95398299
EP 815507	A1	E		G06F-009/00	Based on patent WO 9625705
Designated States (Regional): DE FR GB					
US 5751985	A			G06F-009/30	Cont of application US 95390885
					Cont of application US 95398299
JP 11500551	W		354	G06F-009/38	Based on patent WO 9625705
KR 98702203	A			G06F-009/00	Based on patent WO 9625705
US 5966530	A			G06F-011/00	Cont of application US 95390885
					Cont of application US 95398299
					Div ex application US 95487801
					Div ex patent US 5751985

Abstract (Basic): WO 9625705 A

The method involves defining a data structure in the data store. An identification tag is assigned to each instruction issued by the issue unit. An activity bit stored in the data structure for each instruction is associated based on the assigned tag.

The activity bit in the **data** structure is **set** when the instruction is issued. The activity bit in the data structure is cleared when the instruction completes execution without error.

ADVANTAGE - Performs frequent traps without degrading processor performance.

Dwg.13/60

Title Terms: INSTRUCTION; EXECUTE; TRACK; PROCESSOR; ASSIGN; IDENTIFY; TAG; INSTRUCTION; ISSUE; ASSOCIATE; ACTIVE; BIT; SET; ISSUE; CLEAR; COMPLETE

Derwent Class: T01

International Patent Class (Main): **G06F-007/46 ; G06F-009/00 ; G06F-009/30 ; G06F-009/38 ; G06F-011/00**

International Patent Class (Additional): **G06F-009/30**

File Segment: EPI

20/5/22 (Item 13 from file: 350)

DIALOG(R)File 350:Derwent WPIX

010857255 **Image available**

WPI Acc No: 1996-354208/199635

XRPX Acc No: N96-298758

Computer system performance monitoring method - involves compiling source code into corresponding object code which is in turn translated into link

```
Set     Items   Description
S1      91989   (PROFILE OR EDGE? OR MODULE? OR NODE? OR VERTICE? OR VERTEX
             OR EDGES OR ATOMIC()PROPOSITION? OR ADDRESSABLE()DEVICE? OR -
            SET OR SUBSET OR SUB()SET?)(2N)(CODE OR CODES OR INFORMATION -
            OR DATA)
S2       4687   (BRANCH? OR LEAF OR LEAVES OR STUB OR STUBS OR ROUTINE? OR
            REFERENCE OR FORWARDING)(N)(CODE OR CODES OR INSTRUCTION?)
S3      39252   (EXTERNAL? OR OUTSIDE OR OUT()SIDE OR EXTERIOR? OR INDEPEN-
            DENT?)(2N)( FUNCTION? OR METHOD? OR INSTRUCTION? OR OPERATION?
             OR EXECUTION? OR COMMAND?)
S4      27261   (EXECUT? OR PERFORM? OR TRANSACT?)(3N)CODE? ?
S5    1435356   GENERAT? OR CREAT? OR PRODUC? OR DEVELOP? OR ESTABLISH?
S6    1535681   CONNECT? OR LINK? OR JOIN? OR UNITE? OR UNIFY OR UNIFIES OR
             COMBINE? OR ASSOCIAT? OR AFFILIAT? OR ASSEMBLE? OR TIE? OR C-
            OLLECT?
S7      30600   (PROFILE? OR HISTOR? OR PATTERN? OR ATTRIBUT? OR EDGE)(2N)-
            DATA
S8     956399   HIT OR HITS OR LOCAT? OR FIND? OR MATCH?
S9      37733   (OPEN? OR START? OR BEGIN? OR ENTRY)(N)POINT?
S10     11797   (TARGET? OR INDICAT? OR GOAL? OR DESTINATION)(N)(POINT? OR
            ATTRIBUT?)
S11   1422896   REGISTER? OR RECORD? OR LIST? OR PRESERV? OR SAVE? OR SAVI-
            NG OR KEEP? OR WRITE? OR POST? OR LOG OR LOGGED OR LOGGING OR
            ENTER? ? OR ENTERING
S12    912912   TABLE? OR TUPLE? OR ROW? OR MATRIX OR MATRICES OR ARRAY? OR
             COLUMN? OR GRID? OR GRAPH? OR (MATHEMATICAL OR DATA)()ELEMEN-
            T?
S13     42832   (AFTER OR SUBSEQUENT OR LATER OR FOLLOWING OR SUCCEEDING OR
             SUCCESSIVE OR SEQUENT)(N)(EXECUT? OR PERFORM? OR TRANSACT?)
S14   1503783   ANALYZ? OR ANALYS? OR COMPAR? OR MATCH? OR VERI? OR ANALYZ?
             OR ANALYS? OR LINK? OR SYNCHRON? OR CONFORM? OR AGREE? OR CO-
            MPLIANT OR COMPATIBLE OR DIFFERENT? OR DIFFERENCE? OR SIMILAR?
             OR DISTINGUISH? OR DISCRIMINAT?
S15    890839   MARKER?()BIT? OR INDICAT? OR TAG OR TAGS OR TAGGED OR TAGG-
            ING OR MAPPING OR MAP OR MAPS OR TARGET?
S16         26  S1 (S) S2 (S) S3 (S) S4
S17         20  S16 AND IC=G06F?
File 348:EUROPEAN PATENTS 1978-2004/Jun W02
         (c) 2004 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20040617,UT=20040610
         (c) 2004 WIPO/Univentio
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Set     Items   Description
S1     190867   (PROFILE OR EDGE? OR MODULE? OR NODE? OR VERTICE? OR VERTEX
              OR EDGES OR ATOMIC()PROPOSITION? OR ADDRESSABLE()DEVICE? OR -
             SET OR SUBSET OR SUB()SET?)(2N)(CODE OR CODES OR INFORMATION -
             OR DATA)
S2       2871   (BRANCH? OR LEAF OR LEAVES OR STUB OR STUBS OR ROUTINE? OR
             REFERENCE OR FORWARDING)(N)(CODE OR CODES OR INSTRUCTION?)
S3      73449   (EXTERNAL? OR OUTSIDE OR OUT()SIDE OR EXTERIOR? OR INDEPEN-
             DENT?)(2N)( FUNCTION? OR METHOD? OR INSTRUCTION? OR OPERATION?
              OR EXECUTION? OR COMMAND?)
S4      51271   (EXECUT? OR PERFORM? OR TRANSACT?)(3N)CODE? ?
S5   20120146   GENERAT? OR CREAT? OR PRODUC? OR DEVELOP? OR ESTABLISH?
S6   12224340   CONNECT? OR LINK? OR JOIN? OR UNITE? OR UNIFY OR UNIFIES OR
              COMBINE? OR ASSOCIAT? OR AFFILIAT? OR ASSEMBLE? OR TIE? OR C-
             OLLECT?
S7      83708   (PROFILE? OR HISTOR? OR PATTERN? OR ATTRIBUT? OR EDGE)(2N)-
             DATA
S8    4712960   HIT OR HITS OR LOCAT? OR FIND? OR MATCH?
S9      63563   (OPEN? OR START? OR BEGIN? OR ENTRY)(N)POINT?
S10      8926   (TARGET? OR INDICAT? OR GOAL? OR DESTINATION)(N)(POINT? OR
             ATTRIBUT?)
S11   5412315   REGISTER? OR RECORD? OR LIST? OR PRESERV? OR SAVE? OR SAVI-
             NG OR KEEP? OR WRITE? OR POST? OR LOG OR LOGGED OR LOGGING OR
             ENTER? ? OR ENTERING
S12   5624000   TABLE? OR TUPLE? OR ROW? OR MATRIX OR MATRICES OR ARRAY? OR
              COLUMN? OR GRID? OR GRAPH? OR (MATHEMATICAL OR DATA)()ELEMEN-
             T?
S13     32959   (AFTER OR SUBSEQUENT OR LATER OR FOLLOWING OR SUCCEEDING OR
              SUCCESSIVE OR SEQUENT)(N)(EXECUT? OR PERFORM? OR TRANSACT?)
S14  27953322   ANALYZ? OR ANALYS? OR COMPAR? OR MATCH? OR VERI? OR ANALYZ?
              OR ANALYS? OR LINK? OR SYNCHRON? OR CONFORM? OR AGREE? OR CO-
             MPLIANT OR COMPATIBLE OR DIFFERENT? OR DIFFERENCE? OR SIMILAR?
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